We Claim:

1. A test structure to test tunnel openings in a non-volatile memory cell, comprising:

one or more write paths;

an oxide layer formed over the one or more write paths;

an array of tunnel openings formed in the oxide layer;

multiple floating gates formed over the oxide layer; and

wherein at least one of the write paths has multiple tunnel openings from the array formed thereon.

2. The test structure of claim 1, wherein the array of tunnel openings is of size NxM, where N is the number of write paths and M is the number of floating gates.

3. The test structure of claim 1, wherein at least one of the floating gates is aligned to a subset of tunnel openings from the array so that each tunnel opening in the subset can separately be used to program or erase the floating gate.

4. The test structure of claim 1, wherein at least one write path is electrically coupled to multiple floating gates through multiple tunnel openings.

5. The test structure of claim 4, wherein there is a one-to-one correspondence between tunnel openings in the write path and the floating gates.

6. The test structure of claim 1, wherein at least a first floating gate is electrically coupled to multiple tunnel openings so that the first floating gate is separately programmable and erased through any one of the multiple tunnel openings.

7. The test structure of claim 1, wherein the multiple floating gates are positioned perpendicular to multiple write paths and wherein a tunnel opening is located at each floating gate and write path intersection.

8. The test structure of claim 1, further including a control path coupled to the floating gates and a read path coupled to the floating gates.

9. The test structure of claim 8, wherein the read path and the floating gates form a series of sense devices that are turned ON with the floating gates programmed and that are turned OFF with the floating gates erased.

10. The test structure of claim 1, wherein multiple write paths are perpendicularly aligned to the multiple floating gates and wherein the tunnel openings associated with the write paths vary in size.

11. The test structure of claim 1, wherein a first write path has a one-dimensional array of same size tunnel openings formed thereon, and further including a second write path having a one-dimensional array of same size tunnel openings formed thereon, wherein the tunnel openings on the second write path are designed to be larger than the tunnel openings on the first write path.

12. A test structure for testing tunnel opening sizes, comprising:

multiple write paths aligned in parallel;

multiple floating gates aligned in parallel and aligned perpendicularly to the multiple write paths, the floating gates overlapping the multiple write paths to form an array of intersecting areas where the overlap occurs;

an array of tunnel openings formed in the intersecting areas of overlap; and

wherein at least one of the write paths is electrically coupled to the multiple floating gates through multiple of the tunnel openings to allow programming and erasing of multiple floating gates in parallel.

13. The test structure of claim 12, wherein one tunnel opening is formed in each intersecting area of overlap.

14. The test structure of claim 12, wherein each write path is electrically coupled to the multiple floating gates.

15. The test structure of claim 12, further including a read path aligned perpendicularly to and coupled to the multiple floating gates to form a series of sense transistors.

16. The test structure of claim 12, further including a control path aligned perpendicularly to and coupled to the multiple floating gates to control programming and erasing the multiple floating gates in parallel.

17. The test structure of claim 12, wherein the array of tunnel openings includes rows and columns of tunnel openings, wherein any of the columns have same size tunnel openings associated therewith and wherein each column is associated with a different size of tunnel opening from other columns in order to test varying sizes of tunnel openings.

18. The test structure of claim 12, wherein the multiple write paths are designed to have different size tunnel openings for purposes of testing tunnel openings of varying sizes.

19. The test structure of claim 18, wherein a first write path is associated with a one-dimensional array of a first size tunnel opening and a second write path is associated with a one dimensional array of a second size tunnel opening, which differs in size from the first size.

20. The test structure of claim 19, wherein a first floating gate is electrically coupled to multiple tunnel openings designed to have varying sizes.

21. A test structure to test tunnel openings in a memory cell, comprising:

a plurality of write paths formed in parallel;

an oxide layer adjacent to the write paths;

an array of tunnel openings formed in the oxide layer, the array having multiple rows and columns of multiple tunnel openings; and

wherein at least one of the columns in the array of tunnel openings is electrically coupled with a single write path.

22. The test structure of claim 21, further including a plurality of floating gates, wherein at least one row in the array of tunnel openings is electrically coupled to a single floating gate.

23. A method of testing tunnel opening sizes, comprising:

(a) charging multiple floating gates to a predetermined potential;

(b) reading multiple sense devices to determine whether charge is stored on the floating gates;

(c) with a single write path, removing charge from the multiple floating gates in parallel; and

(d) re-reading the multiple sense devices to determine whether charge is removed from the floating gates.

24. The method of claim 23, wherein the single write path is a first write path and further including repeating (a)-(d) for multiple write paths, one iteration per write path.

25. The method of claim 24, wherein the write paths are designed with different tunnel opening sizes to test varying sizes of the tunnel openings.

26. The method of claim 23, further including electrically coupling multiple tunnel openings to the single write path and using the single write path to test the multiple tunnel openings in parallel.

27. The method of claim 23, further including providing multiple write paths in parallel to the single write path and wherein charging the floating gates includes setting a voltage on a control line to V_{pp} and setting a voltage level on one of the write paths to ground.

28. A method for testing tunnel opening sizes, comprising:

providing an array of tunnel opening sizes wherein the tunnel openings vary in size to test different sizes of tunnel openings;

charging multiple floating gates in parallel;

for a first size tunnel opening being tested, removing the charge from the multiple floating gates in parallel; and

performing a read to determine whether the charge was removed from the multiple floating gates.

29. The method of claim 28, further including providing multiple write paths in parallel, wherein each write path has multiple same size tunnel openings formed therein, and different write paths have different sizes of tunnel openings associated therewith.

30. The method of claim 29, wherein charging multiple floating gates in parallel includes setting a control path to a V_{pp} voltage level and grounding at least one of the write paths.

31. The method of claim 29, wherein removing the charge from the multiple floating gates in parallel includes using tunnel openings associated with a single write path.

32. The method of claim 28, further including providing multiple sense devices in series, one sense device per floating gate and wherein performing a read includes reading the sense devices to determine if the sense devices are switched ON.

33. The method of claim 28, further including repeating the charging of multiple floating gates in parallel and removing the charge from the multiple floating gates to test different sizes of tunnel openings.

34. A test structure for testing tunnel opening sizes, comprising:

means for programming multiple floating gates in parallel;

means for reading whether the multiple floating gates are properly programmed; and

means for erasing the multiple floating gates in parallel using a single write path.

35. The test structure of claim 34, further including means for electrically coupling varying sizes of tunnel openings to the floating gates.

36. The test structure of claim 34, further including means for electrically coupling the single write path to multiple same-size tunnel openings.

37. A test structure for testing tunnel opening sizes, comprising:

an array of tunnel openings aligned in rows and columns;

a plurality of floating gates electrically coupled to the rows of tunnel openings in a one-to-one correspondence so that a floating gate is electrically coupled to a set of two or more tunnel openings; and

a plurality of write paths electrically coupled to the columns of tunnel openings in a one-to-one correspondence.

38. The test structure of claim 37, wherein the tunnel openings in a first column of the array are of the same size and wherein a first write path is electrically coupled to the first column.

39. The test structure of claim 37, wherein the set of tunnel openings is of varying size so that different size tunnel openings can be tested.